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L1	44119	(dual or two) adj port\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:37
L2	14842	(multi or multiple) adj port\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:40
L3	200478	initialize or initialized or initializing or initialization	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:41
L4	870	l3 near status	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:41
L5	2319	configuration near status	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:42
L6	2	l1 same l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:42
L7	13	l1 same l5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:45
L8	0	l2 same l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:45

L9	2	12 same 15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:46
L10	1485	709/213-216.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:46
L11	2757	711/147-153.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:46
L12	8	110 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:47
L13	5	111 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:48
L14	18	110 and 15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:48
L15	23	111 and 15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT ; IBM_TDB	NEAR	ON	2005/01/18 10:48

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[\[Abstract\]](#) [\[PDF Full-Text \(760 KB\)\]](#) IEEE CNF**2 Distributed route initialization algorithms for the Monash Secure RISC Multiprocessor***Fazio, V.J.; Pose, R.D.;*

System Sciences, 1997, Proceedings of the Thirtieth Hawaii International Conference on , Volume: 5 , 7-10 Jan. 1997

Pages:24 - 33 vol.5

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1 An efficient scheme for interprocessor communication using dual-ported RAMs

Jagadish, N.; Kumar, J.M.; Patnaik, L.M.;
Micro, IEEE, Volume: 9, Issue: 5, Oct. 1989
Pages:10 - 19

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2 Codesign system performance based on memory configurations

Mourelle, L. de M.; Nedjah, N.;
Integrated Circuits and Systems Design, 1999. Proceedings. XII Symposium on, 29 Sept.-2 Oct. 1999
Pages:36 - 41

[\[Abstract\]](#) [\[PDF Full-Text \(80 KB\)\]](#) **IEEE CNF**

3 A flexible ServerNet-based fault-tolerant architecture

Baker, W.E.; Horst, R.W.; Sonnier, D.P.; Watson, W.J.;
Fault-Tolerant Computing, 1995. FTCS-25. Digest of Papers., Twenty-Fifth International Symposium on, 27-30 June 1995
Pages:2 - 11

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4 The Concentrated Range Extender with Gain

Henry, J.; Stiefel, K.; Stone, D.; Williamson, D.;
Communications, IEEE Transactions on [legacy, pre - 1988], Volume: 28, Issue: 7, Jul 1980
Pages:943 - 948

[\[Abstract\]](#) [\[PDF Full-Text \(936 KB\)\]](#) **IEEE JNL**

5 A single-chip 1.6 billion 16-b MAC/s multiprocessor DSP

Ackland, B.; Anesko, A.; Brinthaup, D.; Daubert, S.J.; Kalavade, A.; Knobloch, J.; Micca, E.; Moturi, M.; Nicol, C.J.; O'Neill, J.H.; Othmer, J.; Sackinger, E.; Singh, K.J.; Sweet, J.; Terman, C.J.; Williams, J.;